ABSTRACT OF DISCLOSURE

A latch circuit to perform high-speed input and output operations by reducing a load of an input circuit or an output circuit of the latch circuit. The latch circuit includes four or more inverters connected in a loop to hold a signal, a plurality of input terminals respectively connected to different nodes, and a plurality of output terminals respectively connected to different nodes. At least one input terminal of the latch circuit is used for normal operation of the latch circuit, and at least one input terminal is used for a test operation of the latch circuit. Further, at least one output terminal of the latch circuit is used for normal operation of the latch circuit, and at least one output terminal is used for a test operation of the latch circuit. The latch circuit reduces the number of circuit elements at a connecting point of an input terminal of the latch circuit or at a connecting point of an output terminal of the latch circuit. By reducing the number of circuit elements at the input or output connections, a load of the input or output can be reduced, and thereby high-speed input or output can be realized.